

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 1116

Roll No.

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B. Tech.

(Semester-I) Theory Examination, 2012-13

ELECTRONICS ENGINEERING

Time : 3 Hours]

[Total Marks : 100

Note : Attempt questions from each Section as per instruction.

Section-A

Attempt *all* parts of this question. Each part carries 2 marks.

2×10=20

1. (a) If a pure silicon crystal has 1 million free electrons inside it, how many holes does it have? What happens to the number of free electrons and holes, if the ambient temperature increases?
- (b) Define the use of Surge resistor.
- (c) Draw the schematic of Peak-to-Peak detector.
- (d) How is Varactor used?

- (e) Calculate the output voltage appear across R_{load} (in Fig. 1).

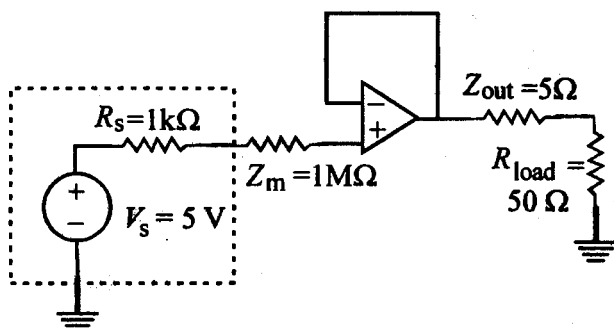


Fig. 1

- (f) Find resistance R_b in Fig. 2 to bring transistor to threshold of saturation $V_{\text{CB}} = 0$, $V_{\text{BE}} = 0.7\text{ V}$, $\alpha = 0.96$.

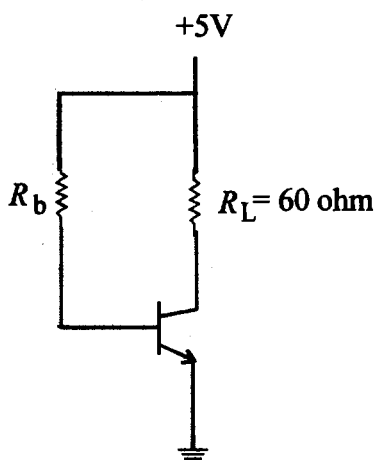


Fig. 2

- (g) MOSFET
- (h) List the primary differences between JFET and MOSFET.
- (i) How to test probes using CRO?
- (j) List the four specifications of DC power supply.

Section-B

Attempt any *three* parts of this question. Each part carries 10 marks. $10 \times 3 = 30$

2. (a) (i) Sketch and explain the circuits of a combination clipper which limit the output between $\pm 10\text{ V}$. Assume the diode voltage is 0.7 V .
- (ii) With neat diagram and waveforms explain the working of a negative clamper and also write the condition for stiff clamper.
- (b) Given $\beta = 50$ for the transistor circuit shown in Fig. 3, find the transistor currents I_C , I_E and I_B . In which region is the transistor operating? Justify.

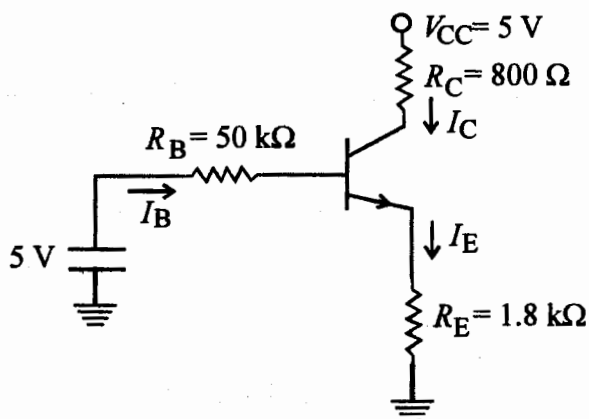


Fig. 3

- (c) Describe the drain curves and transconductance curve of enhancement mode and depletion mode MOSFET. Derive an expression for g_m of JFET configuration.
- (d) Draw the block diagrams of four types of Negative Feedback Amplifiers. Also calculate VCVS voltage gain, input impedance and output impedance.
- (e)
 - (i) Explain, how you would measure phase of signal from C.R.O.
 - (ii) Describe the working of digital multi-meter with neat block diagram.

Section-C

Attempt *all* questions of this Section. Each question carries 10 marks. $10 \times 5 = 50$

3. Attempt any two parts :

- (a) Sketch the waveform output V_{out} in the circuit of Fig. 4, indicating the values of maximum positive and negative output voltages.

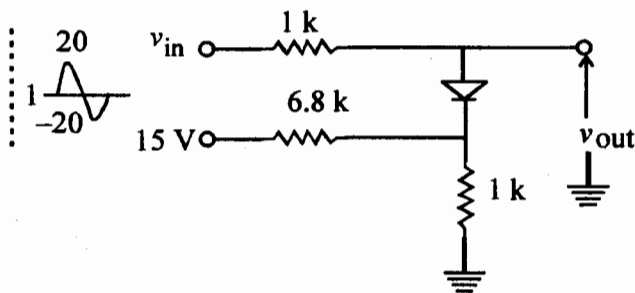


Fig. 4

- (b) Explain the working of Voltage Multiplier.
- (c) Explain the working of Schottky diode.
4. Attempt any two parts :
- (a) Explain the working of an emitter follower circuit with its circuit diagram.

- (b) Draw the schematic of direct couple output stage and explain its working.
 - (c) Compare different types of biasing methods.
5. Attempt any two parts :
- (a) Define Ohmic region, gate cut-off voltage and transconductance in JFET.
 - (b) Draw the schematic of CS JFET amplifier and determine A_v .
 - (c) Explain the active load switching circuit using the MOSFET.
6. Attempt any one part :
- (a) Explain :
 - (i) Input bias current compensation in OPAMP.
 - (ii) Integrator using OPAMP.
 - (iii) Zero crossing detector using OPAMP.
 - (b) (i) Obtain an expression for the closed loop gain of a non-inverting amplifier.
 - (ii) Describe the method of measuring and calculating CMMR of an OPAMP.

7. Attempt any two parts :

- (a) Compare the design issues of analog meters and digital meters.
- (b) Draw the basic block diagram of a function generator and explain the function of each block.
- (c) Explain the procedure to obtain the Lissajous pattern on the screen of a CRO and also explain how the phase of an unknown signal can be determined from it.